APPLICATION FOR UNITED STATES LETTERS PATENT

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TITLE: **RESISTIVE ISOLATION BETWEEN A BODY AND A BODY CONTACT**

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BACKGROUND

[0001] In conventional stacked devices, isolated wells for transistors may be used to reduce the body effect and the corresponding shifts in threshold voltages of the transistors. Despite having such benefits, additional costs of forming isolated wells for transistors render its implementation less desirable. As an alternative, low threshold voltage transistors may be used to reduce the body effect. However, low threshold voltage transistors may respond poorly to signals because of their grounded bodies. With the bodies connected to ground, the performance of transistors (e.g., low threshold voltage transistors) may suffer from the accompanying body effect.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The invention may be understood by referring to the following description and accompanying drawings that are used to illustrate the embodiments of the invention. In the drawings:

FIG. 1 shows a circuit diagram of a device according to an exemplary embodiment of the invention;

FIG. 2 shows a cross-sectional side view of a device according to an exemplary embodiment of the invention;

FIG. 3 shows an upper view of a device according to an exemplary embodiment of the invention;

FIGS. 4A-D show a method according to an exemplary embodiment of the invention;

FIG. 5 shows a gain improvement achieved in a complementary metal-oxide semiconductor (CMOS) power amplifier by using a device according to an exemplary embodiment of the invention;

FIG. 6 shows a device according to another exemplary embodiment of the invention;

FIG. 7 shows a system incorporating a device according to an exemplary embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0003] In the following description, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other circumstances, well known circuits, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

[0004] References to an "exemplary embodiment" indicate that the embodiment(s) of the invention so described may include a particular feature, structure, or characteristic, but not every embodiment necessarily includes the particular feature, structure, or characteristic. Further, repeated use of the phrase "an exemplary embodiment" does not necessarily refer to the same embodiment, although it may.

[0005] In the following description and claims, the terms "coupled" and "connected," along with their derivatives, may be used. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical or electrical contact with each other. "Coupled" may mean that two or more elements are in direct physical or lesser contact. However, "coupled" may also mean that two or more elements are not in direct contact with each other, but they still co-operate or interact with each other.

[0006] In FIG. 1, a device 100 according to an exemplary embodiment of the invention may receive an input signal (e.g., an alternating current (AC) input signal such as a radio frequency (RF) input signal or any other signal) at a control electrode 122 and may output an output signal (e.g., an AC output signal such as an RF output signal or any other signal) at an output node 150. The device 100 may comprise two transistors 110, 120, which may form a cascaded pair (e.g., a cascode amplifier) as depicted in FIG. 1. The body of the upper transistor 110 may be coupled to ground via a resistance 140. The body of the lower transistor 120 may be coupled to ground without an intervening resistance. The resistance 140 may be large enough to substantially isolate the body of the upper transistor 110 from ground, especially when the input signal at the control electrode 122 is at or above a predetermined operating frequency. By having the body of

the upper transistor 110 substantially isolated from ground by the resistance 140, formation of separate wells for the transistors 110, 120 may be obviated. The body and the source of the upper transistor 110 may be coupled to each other by a parasitic source-body capacitance of the upper transistor 110. The parasitic source-body capacitance of the transistors 110, 120 may be a depletion type. A discrete capacitance 160 may optionally be added between the source and the body of the transistor 110, in addition to the parasitic source-body capacitance, to improve the coupling therebetween. With the body isolation from ground, the upper transistor 110 may have an improved response to signals applied to the upper transistor 110 and may exhibit an improved transistor gain.

[0007] The lower transistor 120 may receive the input signal at the control electrode 122. The upper transistor 110 may receive a bias voltage Vbias and may be coupled to a load 130 and may output an output signal at an output node 150. The load 130 may be any type of load, including, but not limited to, an inductance, a resistance, a capacitance and a combination of load types. The bias voltage Vbias may be any reference voltage that biases the upper transistor 110 in a desired state, including a constant or variable voltage. A variable voltage used for this purpose may be set at a selected voltage level before the operation of the device 100 or may vary during the operation of the device 100. When the input signal is applied to the control electrode 122 of the transistor 120, the input signal may be amplified by a gain of the device 100 (i.e., a device gain determined by the transistors 120, 110, the bias voltage Vbias, and the load 130) to provide the output signal at the output node 150.

[0008] The device 100 may be implemented with n-type transistors as depicted. Alternatively, the device 100 may be implemented with p-type transistors by using any of the conventional ways of converting an n-type transistor circuit to a p-type transistor circuit. For example, the device 100 may also be implemented with p-type transistors by using p-type transistors in place of the n-type transistors and switching the polarity of the power supply voltage.

[0009] In FIG. 2, a partial cross-sectional side view of the transistors 110, 120 in FIG. 1 according to an exemplary embodiment of the invention is shown. A substrate 210, a layer 220 on top of the substrate, and the transistors 110, 120 formed in the layer 220 are shown. The layer 220 may be an epitaxial layer formed on the substrate 210. The

substrate 210 and the layer 220 may be formed of a same conductivity type material (e.g., p-type conductivity). When first made, each of the substrate 210 and the layer 220 may have little or no impurity. Thus, each of the substrate 210 and the layer 220 may have a relatively high resistivity. After the initial manufacturing, either or both of the substrate 210 and the layer 220 may be doped with impurities to raise the impurity concentration of the respective layer.

[0010] The transistor 110 may have a drain 212, a source 214 and a gate 219. Each of the drain 212 and the source 214 of the transistor 110 may have a contact, 216 and 218, respectively. The transistor 110 may be surrounded by a high-resistance region 240, which reflects the resistance 140 of FIG. 1. Similar to the transistor 110, the transistor 120 may have a drain 222, a source 224 and a gate 229. Each of the drain 222 and the source 224 of the transistor 120 may be coupled to a contact, 226 and 228, respectively. The gates 219, 229 and the contacts 216, 218, 252, 226, and 228 may be formed of any gate/contact material including, but not limited to, metal and poly silicon. A body 223 of the transistor 120 may be coupled to a body contact region 250. The body contact region 250 may form a distinct or integrated region in the body 223 of the second transistor 120, and may be coupled to a contact 252. The magnitude of the intervening high-resistance region 240 may be high enough to substantially isolate the body 213 of the first transistor 110 from the body contact region 250 without having to create the transistor in its own well.

[0011] The high-resistance region 240 may be formed in the layer 220, for example, by masking and blocking a region 240 of the layer 220 from a subsequent impurity doping of the layer 220. Thus, the impurity concentration of the high-resistance region 240 of the layer 220 may be lower than an impurity concentration of the unmasked regions of the first layer 220. By having a lower impurity concentration, the high-resistance region 240 may have a resistivity higher than the unmasked regions of the layer 220. Any other known method of creating a resistance may also be used in forming the high-resistance region 240 as long as the overall resistance between the body 213 of the upper transistor 110 and the body contact region 250 is increased. The high-resistance region 240 of the resistance 140 may extend over substantially an entire cross-sectional area of the first layer 220 between the body 213 of the transistor 110 and the

body contact region 250 and, thus, may avoid any shunt resistance being created across the high-resistance region 240. The value of the effective resistance 140 due to the high-resistance region 240 may be constant throughout the high-resistance region 240 or may vary. Similarly, the impurity concentration may be constant throughout the resistance region 240 or may vary.

[0012] In FIG. 3, a partial upper view of transistors 110, 120 in FIG. 1 according to an exemplary embodiment of the invention is shown. The high-resistance region 240 of the transistor 110 may surround the transistor 110 as depicted to substantially isolate the body 213 of the transistor 110 from the body contact region 250. Alternatively, the high-resistance region 240 may not surround the transistor 110 completely. If the transistors are laid out differently from the layout of FIG. 3, the body 213 of the transistor 110 may be substantially isolated from the body contact region 250 without having the high-resistance region 240 surround the transistor 110 completely.

[0013] As shown in FIG. 2, the body 223 of the transistor 120 may be coupled to the body contact region 250 without an intervening resistance. Alternatively, the body 223 of the transistor 120 may be coupled to the body contact region 250 with an intervening resistance. Transistors other than the transistors 110, 120 may have their bodies coupled to the body contact region 250 with or without an intervening resistance.

[0014] In FIGS. 4A-D, a method of creating a resistance according to an exemplary embodiment of the invention is shown. In FIGS. 4A and 4B, layer 220 may be formed or placed on top of substrate 210. In FIG. 4C, a mask 410 may be placed over a region 240 of the layer 220 corresponding to a high-resistance region to be created. The layer 220 may be implanted with impurities as shown by the arrows while the mask 410 is placed over the region 240. The region 240 may be blocked from being implanted with impurities by the mask 410 to create a high-resistance region 240 having a lower impurity concentration than the unmasked regions of the layer 220. In FIG. 4D, when the mask 410 is removed, the region 240 may then have a lower impurity concentration (and thus, a higher resistance) than unmasked regions of the layer 220. The high-resistance region 240 may be created in any region where a resistance is desired including, but not limited to, a region between a body of a transistor and a body contact region and a region

between two transistors (e.g., field-effect transistors (FETs) and bipolar-junction transistors (BJTs)).

[0015] In FIG. 5, a gain improvement achieved in a CMOS power amplifier using the device 100 of FIG. 1 according to an embodiment of the invention is shown. By having the body resistance 140 formed between the body of the transistor 110 and ground, the gain of the CMOS power amplifier incorporating the device 100 of FIG. 1 may be improved by as much as 3.4 dB, although various embodiments of the invention are not limited in this respect. Such gain may correspond to more than doubling the gain of the CMOS power amplifier, for example. The peak efficiency of the CMOS power amplifier may improve from, for example, 28.5% to 30.7%; such improvement in the peak efficiency may be significant in a power amplifier where a lower efficiency represents a significant waste of power.

[0016] In FIG. 6, a device 100' with p-type transistors 110', 120' having a body coupled to a power supply via a body resistance 140' according to another exemplary embodiment of the invention is shown. The embodiment of the device 100' in FIG. 6 may be physically analogous to and may operate in a similar way to the embodiment of the device 100 in FIG. 1. As shown in FIG. 6, p-type transistors 110', 120' may be used in place of the n-type transistors in FIG. 1, a polarity of the power supply is changed, and a body of the p-type transistor 110' may be coupled to a power supply via the body resistance 140'. Other known and/or yet to be discovered ways of converting an n-type circuit to a p-type circuit may also be used.

[0017] In FIG. 7, a system using the device 100 according to an exemplary embodiment of the invention is shown. The device 100 may receive an input signal from a signal generating device 710 and may output an output signal to an output device 720. The signal generating device 710 may be any device that produces an input signal including, but not limited to, a data source, a signal generator, a modulator, a receiver or a transceiver, and the output device 720 may be, but is not limited to, a load, such as an antenna, including radio frequency devices and omnidirectional antennas.

[0018] The exemplary embodiments shown in FIGS. 1-6 may also be used in any system or device including, but not limited to, power amplifiers (e.g., power amplifiers in advanced CMOS processes with lower operating voltages), highly integrated transceivers

for wireless local area networks (LANs) (e.g., an RF wireless LAN) and mobile phone applications.

[0019] The foregoing description is intended to be illustrative and not limiting. Variations will occur to those of skill in the art. Those variations are intended to be included in the various embodiments of the invention, which are limited only by the spirit and the scope of the appended claims.